Serial Number: 10/621,253

Filing Date: July 14, 2003

Title: STRUCTURAL REGULARITY EXTRACTION AND FLOORPLANNING IN DATAPATH CIRCUITS USING VECTORS

Assignee: Intel Corporation

## IN THE ABSTRACT OF THE DISCLOSURE

The abstract is objected to because it includes more than 150 words.

Please amend the Abstract as follows:

In some embodiments, a computer-aided design system comprises a functional regularity extraction component, a structural regularity extraction component and a floorplanning component. The functional regularity extraction component provides a method to extract regularity for circuits (and in particular datapath circuits) based on the functional characteristics of a logic design. Some embodiments of the functional regularity extraction component automatically generate a set of templates to cover a circuit. A template is a representation of a subcircuit with at least two instances in the circuit. The templates generated by the functional regularity extraction component are used by a structural regularity extraction component. The structural regularity extraction component provides a method to extract regularity for circuits (and in particular datapath circuits) based on the structural characteristics of a logic design. Some embodiments of the structural regularity extraction component automatically generate a set of vectors for the logic design. A vector is a group of template instances that are identical in function and in structure. The vectors generated by the structural regularity extraction component are used by a floorplanning component. The floorplanning component provides a method of generating a circuit layout from the set of vectors. In some embodiments, each vectors corresponds to a row in the circuit layout.